

**REMARKS/ARGUMENTS**

Reconsideration of this application is requested. Claims 1-46 remain in the application. Claim 15 has been editorially amended. Claim 37 has been amended by adding the step of writing the bits read from the internal matrix to an output matrix, which was previously in claim 45. Claim 45 has been amended to delete that step.

In Section 3 of the Detailed Action portion of the Office Action, claims 37-41 and 43-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Kroeger et al. (US 6,345,377).

Kroeger et al. was cited as shown in figures 3-5, a method for interleaving bits of a digital signal in a digital audio broadcasting (DAB) system comprising writing bits into matrix in the form of partitions and reading bits from the matrix and mapping the partitions into frequency partitions (carriers) for OFDM communications, also citing column 3, lines 60-65 and column 6, line 58 to column 10, line 28.

This rejection is traversed. The Applicant respectfully submits that the amended claims contain features that are neither disclosed nor suggested by Kroeger et al. In particular, independent claim 37 includes the steps of writing a plurality of bits of the digital signal to an internal matrix *in a convolutional interleaver*, wherein the plurality of bits are arranged in a plurality of interleaver partitions, reading the bits from the internal matrix, and writing the bits read from the internal matrix to an output matrix.

Kroeger et al. discloses a digital audio broadcasting system that uses block interleaving. In the system of Kroeger et al., bits are written into a matrix in partitions, which are divided into blocks (col. 9, lines 36-39). Then the bits are read from the same matrix and mapped to frequency partitions in an OFDM signal. Only a single matrix is used. Kroeger et al. does not disclose or suggest a convolutional interleaver or an interleaver having an internal matrix and an output matrix.

The present invention as defined in claim 37 includes the use of a convolutional interleaver wherein a plurality of bits are arranged in a plurality of interleaver partitions, and the bits are mapped from the interleaver partitions to frequency partitions in a radio signal. A convolutional interleaver can be implemented without the need for block synchronization information that is required in a block interleaver. The

Applicant respectfully submits that Kroeger et al. does not disclose or suggest a convolutional interleaver or an interleaver having an internal matrix and an output matrix.

In Section 5 of the Detailed Action portion of the Office Action, claims 1-36 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kroeger et al (US 6,345,377; art cited by applicant) in view of Partyka (US 5,659,580).

Regarding claims 1-36 and 42, Kroeger et al. was cited as teaching the subject matter claimed except for at least one of the writing and reading follows non-sequential addressing scheme. However, Partyka was cited as teaching an interleaver, which follows the non-contiguous (non-sequential) addressing scheme (citing column 2, lines 27-42 and column 4, lines 38-59. According to the Office Action, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kroeger et al. by using the addressing scheme for the interleaving as taught by Partyka so as to simplify the implementation of the interleaver and increase the reliability and the speed of the interleaver circuit.

This rejection is traversed. The Applicant respectfully submits that each of the independent claims contains features that are neither disclosed nor suggested by the cited references. More particularly, each of the Applicant's claims includes an internal matrix and an output matrix, wherein at least one of the steps of writing and reading to or from the internal matrix follows a non-sequential addressing scheme.

The Applicant's invention relates to convolutional interleavers that use a non-sequential addressing scheme. As discussed in the application in paragraph [0167], when the total number of bits being interleaved is greater than the transfer frame size, an additional matrix is used to manage the data flow.

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Partyka also discloses a block interleaver in which blocks of data are interleaved. More particularly, Partyka refers to the IS95 standard, which specifies the use of a block interleaver. Partyka further refers to block interleaving in column 3, at lines 55-56 and in column 4, at lines 38-40. Block interleaving does not require two matrices.

Even if the addressing scheme of Partyka were used with the matrix of Kroeger et al., the combination would not result in the Applicant's invention. The cited references do not disclose or suggest an interleaver having an internal matrix and an output matrix. The Applicant's convolutional interleaver provides the advantage that it can be implemented without the need for block synchronization information that is required in a block interleaver.

The dependent claims include additional features that are not disclosed or suggested by the cited references. For example, claim 2 specifies that the number of bits in the output matrix is equal to the number of bits in a transfer frame of the digital signal. Since the cited references do not disclose or suggest the use of an internal matrix and an output matrix, they do not suggest that the number of bits in the output matrix can be equal to the number of bits in a transfer frame of the digital signal.

In summary, neither Partyka nor Kroeger et al. disclose or suggest an interleaver having an internal matrix and an output matrix, as recited in each of the Applicant's independent claims.

All claims in the application are believed to be allowable. An early Notice of Allowance is requested.

Respectfully submitted,

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